



PTO/SB/08B (08-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Application Number	09/886,959
	Filing Date	June 20, 2001
	First Named Inventor	Algirdas Avizienis
	Art Unit	2114
	Examiner Name	Bryce P. Bonzo
Sheet 1 of 3	Attorney Docket Number	xAAA-02 Technology Center 2600

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
BPB	1	INTEL CORP., Intel's Quality System Databook (January 1998), Order No. 210997-007	
	2	A. AVIZIENIS and Y. HE, "Microprocessor entomology: A taxonomy of design faults in COTS microprocessors", in J. Rushby and [contin'd in next block]	
		C. B. Weinstock, editors, Dependable Computing for Critical Applications 7, IEEE Computer Society Press (1999)	
	3	A. AVIZIENIS and J. P. J. KELLY, "Fault tolerance by design diversity: concepts and experiments", Computer, 17(8):67-80 (August 1984)	
	4	A. AVIZIENIS, "The N-version approach to fault-tolerant software", IEEE Trans. Software Eng., SE11(12):1491-1501 (December 1985)	
	5	M. K. JOSEPH and A. AVIZIENIS, "Software fault tolerance and computer security: A shared problem", in Proc. of the [contin'd in next block]	
		Annual National Joint Conference and Tutorial on Software Quality and Reliability, pages 428-36 (March 1989)	
	6	Y. HE, An Investigation of Commercial Off-the-Shelf (COTS) Based Fault Tolerance, PhD thesis, Computer Science [contin'd in next block]	
		Department, University of California, Los Angeles (September 1999)	
	7	[Please see next sheet.]	

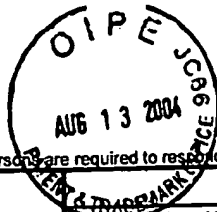
Examiner Signature	Bryce P. Bonzo	Date Considered	7/9/05
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BPB	7	Y. HE and A. AVIZIENIS, "Assessment of the applicability of COTS microprocessors in high-confidence computing [contin'd in next block]	
		systems: A case study", in Proceedings of ICDSN 2000 (June 2000)	
	8	INTEL CORP., The Pentium II Xeon Processor Server Platform System Management Guide (June 1998), Order No. 243835 001	
	9	A. AVIZIENIS, G. C. GILLEY, F. P. MATHUR, D. A. RENNELS, J. A. ROHR, and D. K. RUBIN. "The STAR (Self- [contin'd in next block]	
		Testing-and-Repairing) computer: An investigation of the theory and practice of fault-tolerant computer design", IEEE Trans. [contin'd again]	
		Comp., C 20(11):1312-21 (November 1971)	
	10	T. B. SMITH, "Fault-tolerant clocking system", in Digest of FTCS-11, pages 262-64 (June 1981)	
	11	INTEL CORP., P6 Family Of Processors Hardware Developer's Manual (September 1998), Order No. 244001 001	
	12	A. AVIZIENIS, "Toward systematic design of fault-tolerant systems", Computer, 30(4):51-58 (April 1997)	
7	13	[Please see next sheet.]	

Examiner Signature

Bryce P. Bonzo

Date Considered

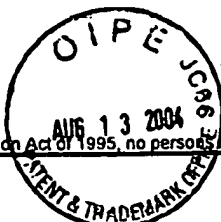
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BPB	13	"Special report: Sending astronauts to Mars", Scientific American, 282 (3):40-63 (March 2000)	
I	14	NASA, "Conference on enabling technology and required scientific developments for interstellar missions", OSS [contin'd in next block]	
▽		Advanced Concepts Newsletter, page 3 (March 1999)	

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